FIG. 1A
(PRIOR ART)

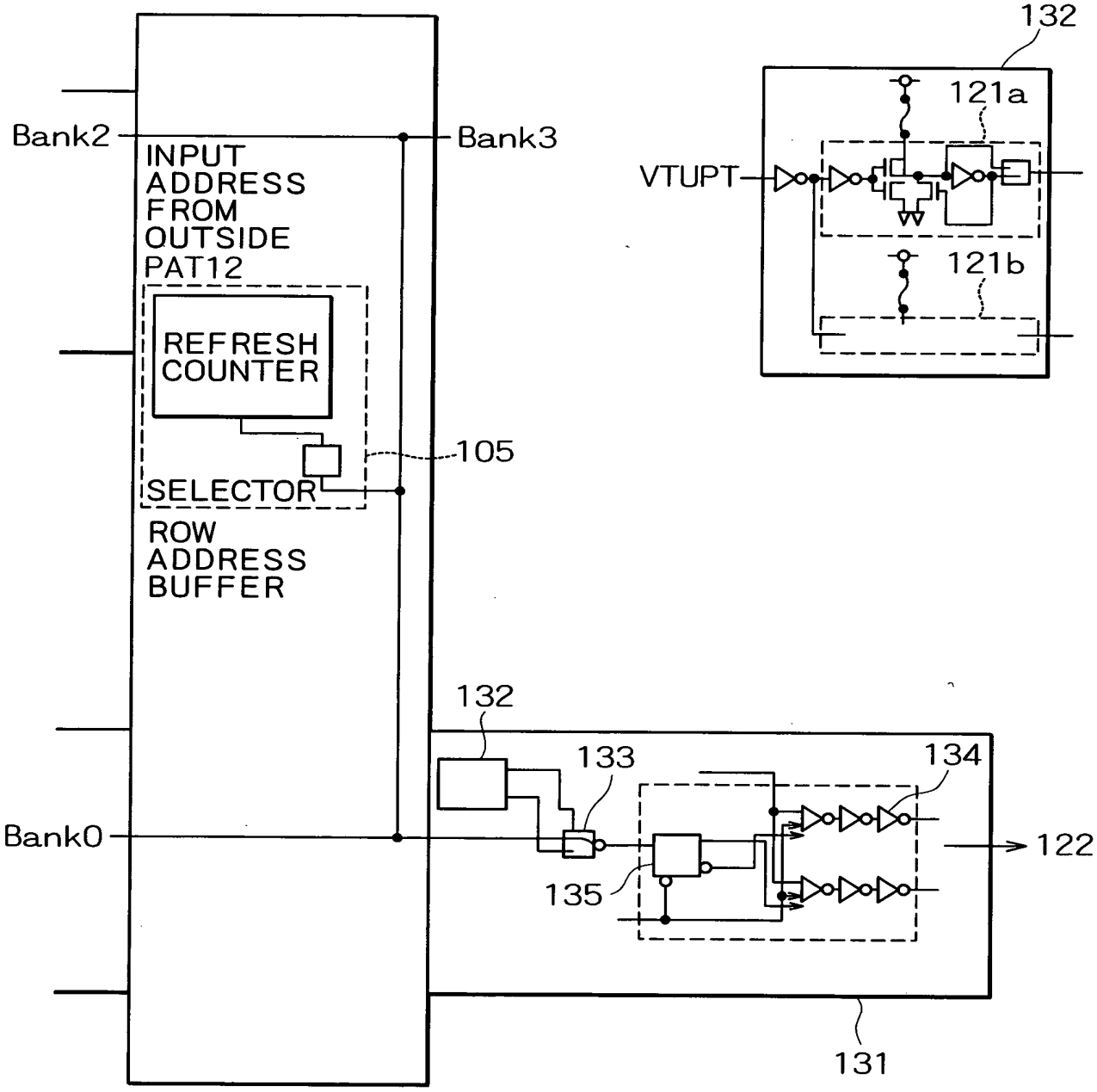

FIG. 1B
(PRIOR ART)

FIG. 2

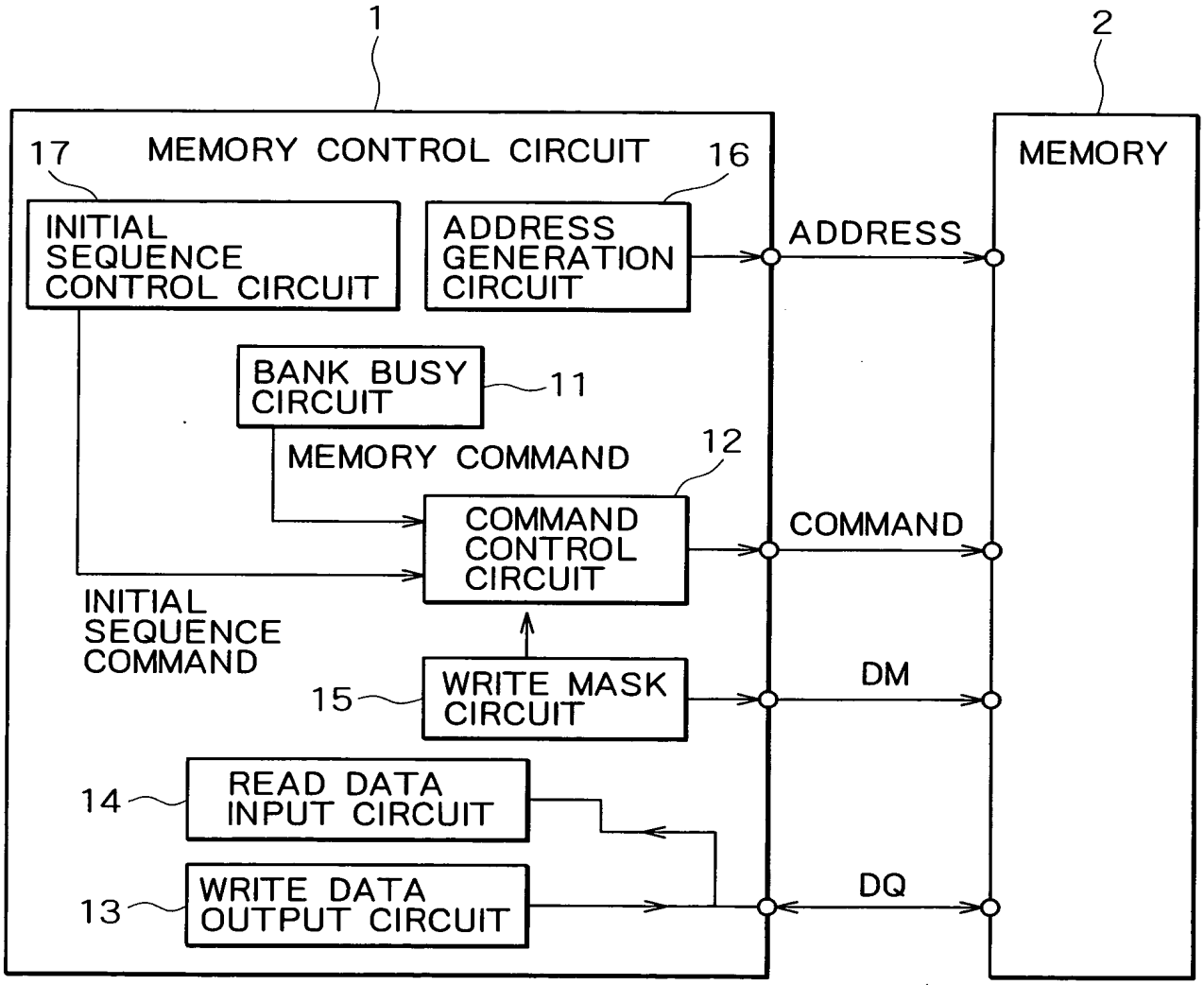
1
2
17
MEMORY CONTROL CIRCUIT
16
MEMORY
INITIAL SEQUENCE CONTROL CIRCUIT
ADDRESS GENERATION CIRCUIT
ADDRESS
BANK BUSY CIRCUIT
11
MEMORY COMMAND
12
COMMAND CONTROL CIRCUIT
COMMAND
INITIAL SEQUENCE COMMAND
15
WRITE MASK CIRCUIT
DM
14
READ DATA INPUT CIRCUIT
13
WRITE DATA OUTPUT CIRCUIT
DQ

FIG. 3

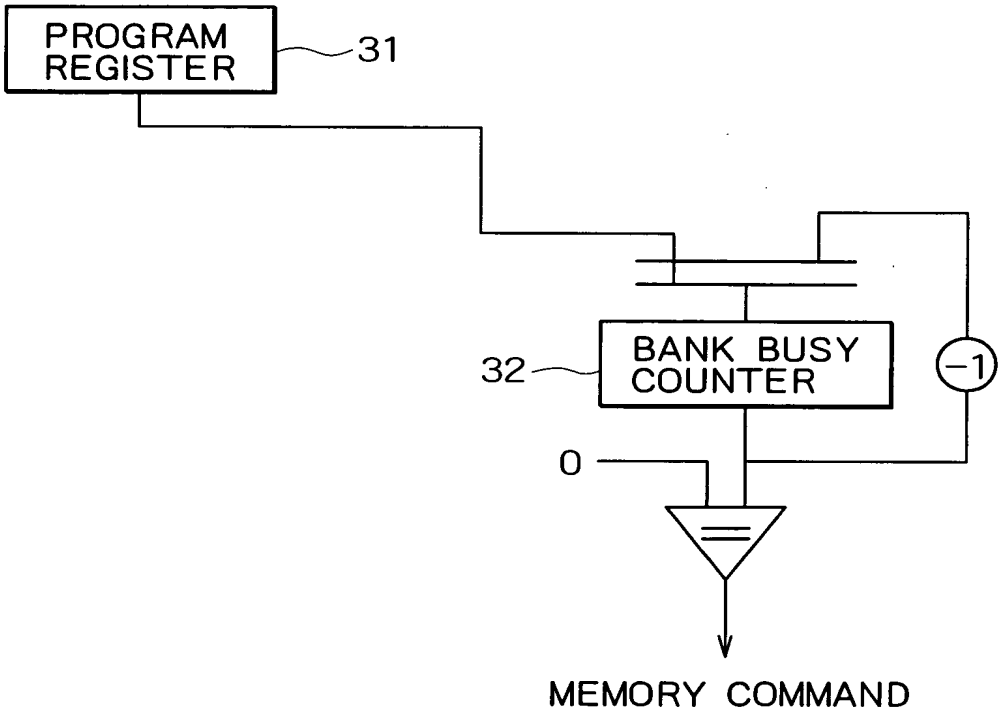

FIG. 4

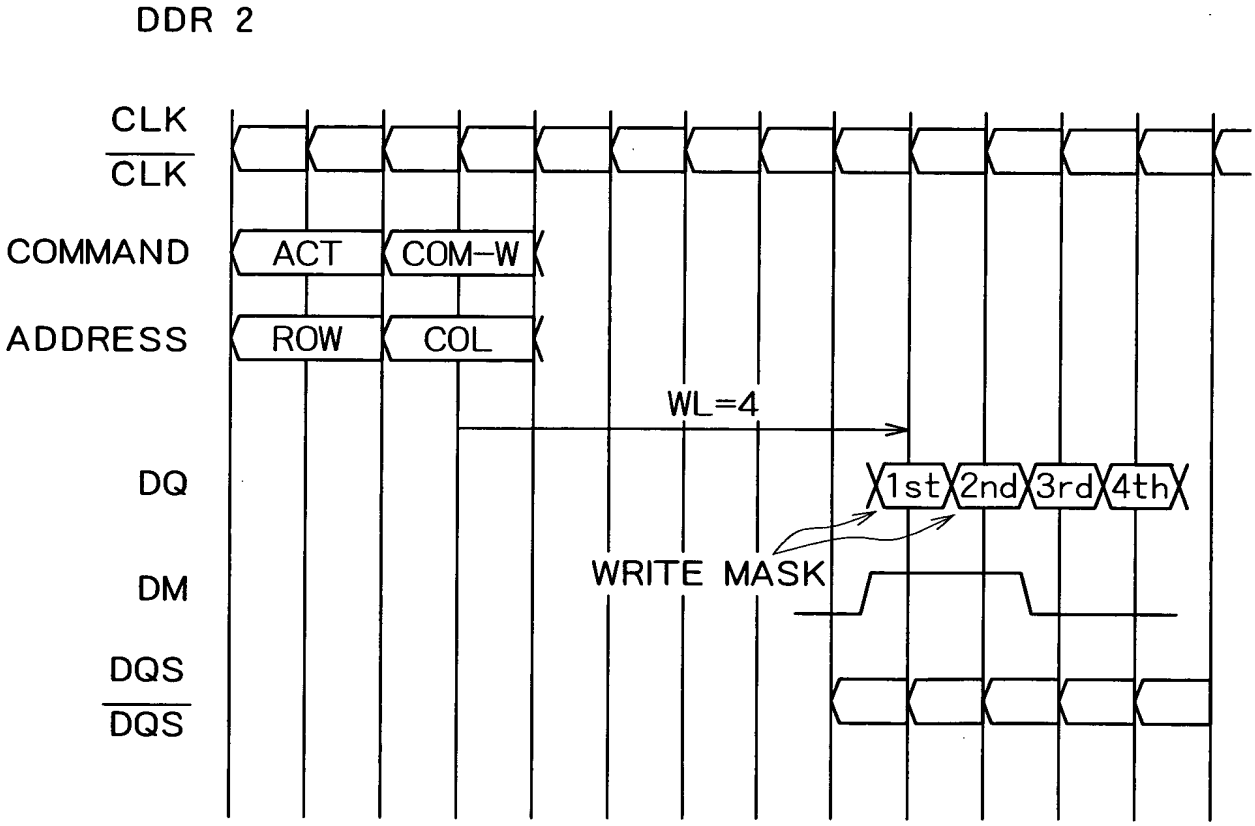
DDR 2
CLK
CLK
COMMAND
ACT
COM-W
ADDRESS
ROW
COL
WL=4
DQ
1st
2nd
3rd
4th
WRITE MASK
DM
DQS
DQS

FIG. 5

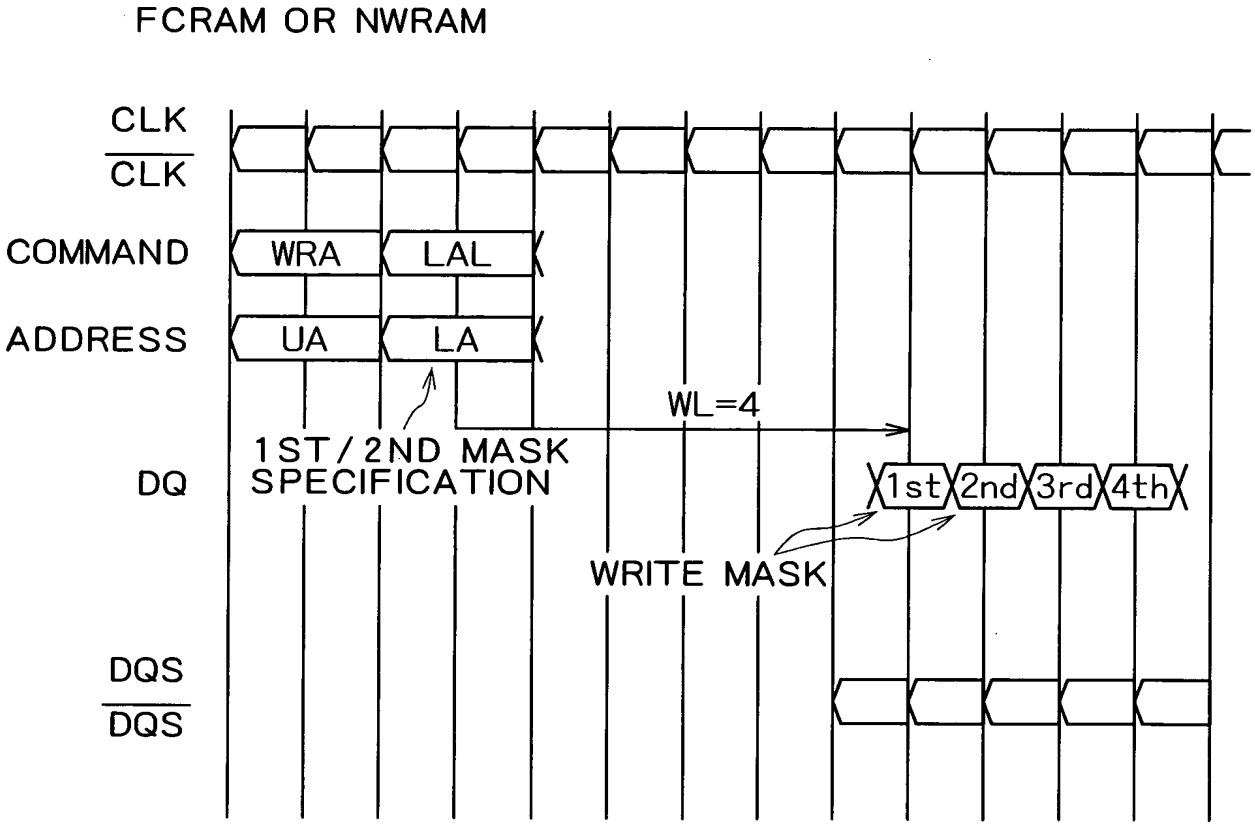
FCRAM OR NWRAM
CLK
CLK
COMMAND
WRA
LAL
ADDRESS
UA
LA
WL=4
1ST/2ND MASK
SPECIFICATION
DQ
1st
2nd
3rd
4th
WRITE MASK
DQS
DQS

FIG. 6

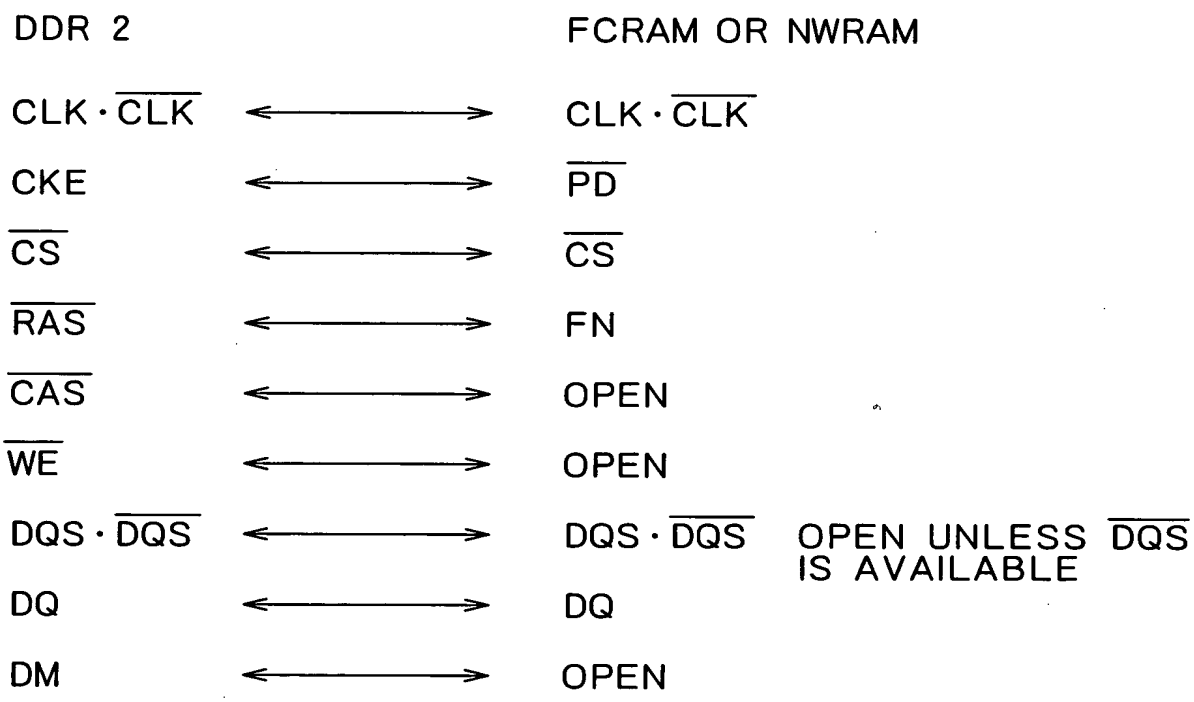
DDR 2
FCRAM OR NWRAM
CLK · $\overline{CLK}$
CLK · $\overline{CLK}$
CKE
$\overline{PD}$
$\overline{CS}$
$\overline{CS}$
$\overline{RAS}$
FN
$\overline{CAS}$
OPEN
$\overline{WE}$
OPEN
DQS · $\overline{DQS}$
DQS · $\overline{DQS}$
OPEN UNLESS $\overline{DQS}$ IS AVAILABLE
DQ
DQ
DM
OPEN

FIG. 7

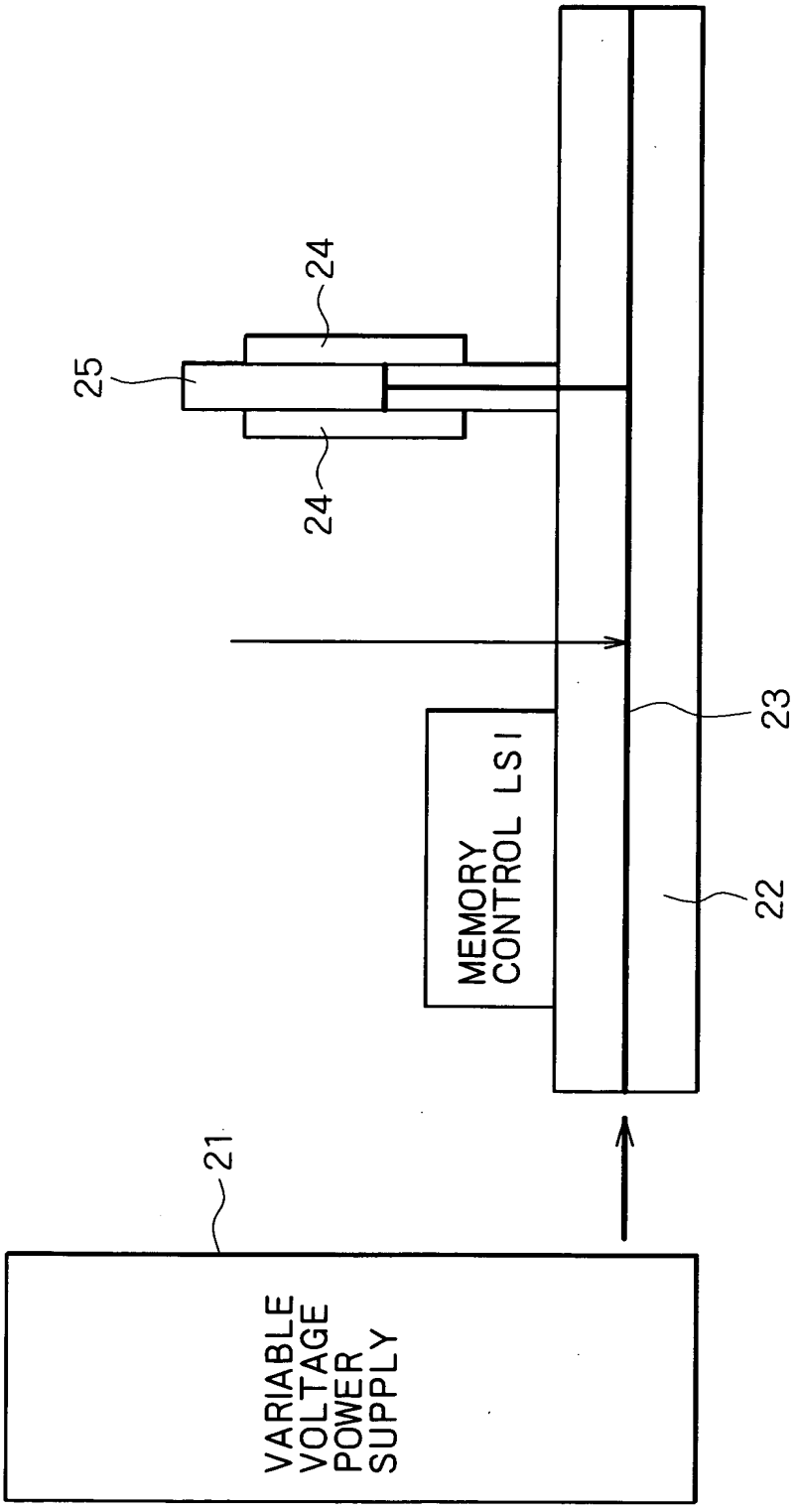
24
25
24
23
MEMORY CONTROL LSI
22
21
VARIABLE VOLTAGE POWER SUPPLY

FIG.8

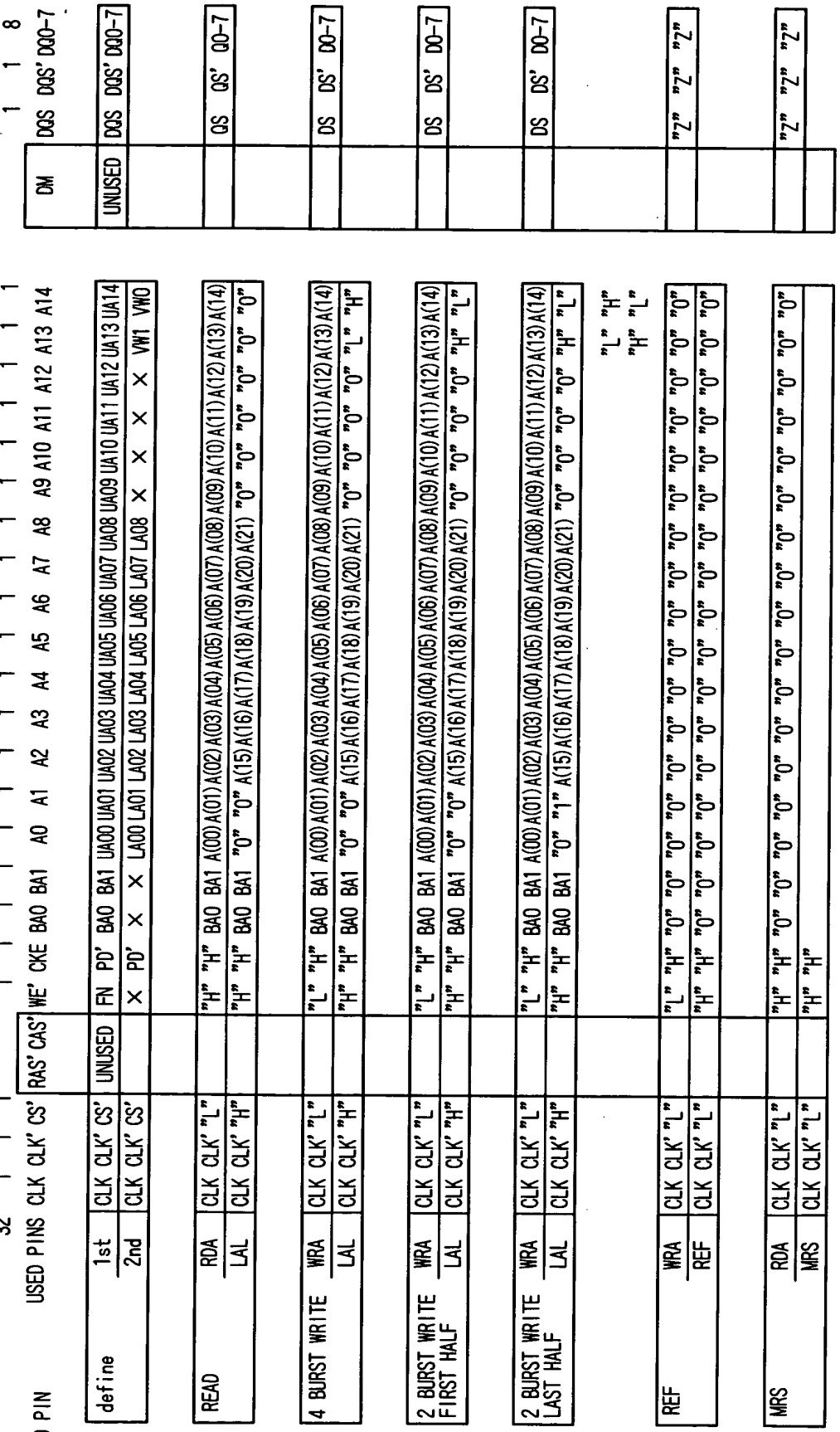
I/O PIN
USED PINS
32 1 1 1 1
CLK CLK' CS'
RAS' CAS' WE' CKE BA0 BA1 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
DM DQS DQS' DQ0-7
1 1 1 8
define 1st CLK CLK' CS' UNUSED FN PD' BA0 BA1 UA00 UA01 UA02 UA03 UA04 UA05 UA06 UA07 UA08 UA09 UA10 UA11 UA12 UA13 UA14
2nd CLK CLK' CS' × PD' × × LA00 LA01 LA02 LA03 LA04 LA05 LA06 LA07 LA08 × × × × VW1 VW0
READ RDA CLK CLK' "L" "H" "H" BA0 BA1 A(00) A(01) A(02) A(03) A(04) A(05) A(06) A(07) A(08) A(09) A(10) A(11) A(12) A(13) A(14)
LAL CLK CLK' "H" "H" "H" BA0 BA1 "0" "0" A(15) A(16) A(17) A(18) A(19) A(20) A(21) "0" "0" "0" "0" "0" "0"
4 BURST WRITE WRA CLK CLK' "L" "L" "H" BA0 BA1 A(00) A(01) A(02) A(03) A(04) A(05) A(06) A(07) A(08) A(09) A(10) A(11) A(12) A(13) A(14)
LAL CLK CLK' "H" "H" "H" BA0 BA1 "0" "0" A(15) A(16) A(17) A(18) A(19) A(20) A(21) "0" "0" "0" "0" "L" "H"
2 BURST WRITE FIRST HALF WRA CLK CLK' "L" "L" "H" BA0 BA1 A(00) A(01) A(02) A(03) A(04) A(05) A(06) A(07) A(08) A(09) A(10) A(11) A(12) A(13) A(14)
LAL CLK CLK' "H" "H" "H" BA0 BA1 "0" "0" A(15) A(16) A(17) A(18) A(19) A(20) A(21) "0" "0" "0" "0" "H" "L"
2 BURST WRITE LAST HALF WRA CLK CLK' "L" "L" "H" BA0 BA1 A(00) A(01) A(02) A(03) A(04) A(05) A(06) A(07) A(08) A(09) A(10) A(11) A(12) A(13) A(14)
LAL CLK CLK' "H" "H" "H" BA0 BA1 "0" "1" A(15) A(16) A(17) A(18) A(19) A(20) A(21) "0" "0" "0" "0" "H" "L"
"L" "H"
"H" "L"
REF WRA CLK CLK' "L" "L" "H" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "Z" "Z" "Z"
REF CLK CLK' "L" "H" "H" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "Z" "Z" "Z"
MRS RDA CLK CLK' "L" "H" "H" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "Z" "Z" "Z"
MRS CLK CLK' "L" "H" "H" "0"

FIG. 9

I/O PIN		34 USED PINS	1 CLK	1 CLK'	1 CS'	1 RAS'	1 CAS'	1 WE'	1 CKE	1 BA0	1 BA1	1 A0	1 A1	1 A2	1 A3	1 A4	1 A5	1 A6	1 A7	1 A8	1 A9	1 A10	1 A11	1 A12	1 A13	1 A14	1 DM	1 DQS	1 DQS'	8 DQ0-7
define	1st	CLK	CLK'	CS'	RAS'	CAS'	WE'	CKE	BA0	BA1	RA00	RA01	RA02	RA03	RA04	RA05	RA06	RA07	RA08	RA09	RA10	RA11	RA12	RA13	UNUSED	DM	DQS	DQS'	DQ0-7
	2nd	CLK	CLK'	CS'	RAS'	CAS'	WE'	CKE	BA0	BA1	LA00	LA01	CA02	CA03	CA04	CA05	CA06	CA07	CA08	CA09	AP	×	×	×					
READ	ACT	CLK	CLK'	"L"	"L"	"H"	"H"	"H"	BA0	BA1	A(00)	A(01)	A(02)	A(03)	A(04)	A(05)	A(06)	A(07)	A(08)	A(09)	A(10)	A(11)	A(12)	A(13)		"L"	QS	QS'	Q0-7
	RDA	CLK	CLK'	"L"	"H"	"L"	"H"	"H"	BA0	BA1	"0"	"0"	A(14)	A(15)	A(16)	A(17)	A(18)	A(19)	A(20)	A(21)	"H"	"0"	"0"	"0"					
4 BURST WRITE	ACT	CLK	CLK'	"L"	"L"	"H"	"H"	"H"	BA0	BA1	A(00)	A(01)	A(02)	A(03)	A(04)	A(05)	A(06)	A(07)	A(08)	A(09)	A(10)	A(11)	A(12)	A(13)		"L"	DS	DS'	Q0-7
	WTA	CLK	CLK'	"L"	"H"	"L"	"L"	"H"	BA0	BA1	"0"	"0"	A(14)	A(15)	A(16)	A(17)	A(18)	A(19)	A(20)	A(21)	"H"	"0"	"0"	"0"					
4 BURST WRITE FIRST HALF	ACT	CLK	CLK'	"L"	"L"	"H"	"H"	"H"	BA0	BA1	A(00)	A(01)	A(02)	A(03)	A(04)	A(05)	A(06)	A(07)	A(08)	A(09)	A(10)	A(11)	A(12)	A(13)		"L→H"	DS	DS'	Q0-7
	WTA	CLK	CLK'	"L"	"H"	"L"	"L"	"H"	BA0	BA1	"0"	"0"	A(14)	A(15)	A(16)	A(17)	A(18)	A(19)	A(20)	A(21)	"H"	"0"	"0"	"0"					
4 BURST WRITE LAST HALF	ACT	CLK	CLK'	"L"	"L"	"H"	"H"	"H"	BA0	BA1	A(00)	A(01)	A(02)	A(03)	A(04)	A(05)	A(06)	A(07)	A(08)	A(09)	A(10)	A(11)	A(12)	A(13)		"H→L"	DS	DS'	Q0-7
	WTA	CLK	CLK'	"L"	"H"	"L"	"L"	"H"	BA0	BA1	"0"	"0"	A(14)	A(15)	A(16)	A(17)	A(18)	A(19)	A(20)	A(21)	"H"	"0"	"0"	"0"					
REF	REF	CLK	CLK'	"L"	"L"	"L"	"H"	"H"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"		"L"	"Z"	"Z"	"Z"
MRS	MRS	CLK	CLK'	"L"	"L"	"L"	"L"	"H"																		"L"	"Z"	"Z"	"Z"

Hisashi ISHIKAWA
"Semiconductor Memory Device and Mount-Type Semiconductor Device"
Q79066---Filed December 24, 2003----Sheets 9 of 9